In the Specification

Page 8, lines 11 and 12 had numbers "216" and "218" swapped, the first full paragraph of page 8 is therefore amended, as follows:

--- The NCO 204 is preferably a 24-bit unsigned adder that adds a variable NCO_VALUE 212 each master clock. For each MCLK of the 27.456MHz clock 208, the NCO 204 adds the NCO_VALUE 212 to the previous value. A frequency signal 214 produced by the NCO 204 is a function of the NCO_VALUE. The circuit converts the MCLK to the desired frequency. NCO_VALUE (bits) = desired frequency (Hz) * 2^{24} (bits) / MCLK (Hz). The top 4-bits of the NCO are used in a digital delay 216 to produce a 16-bit phase sine variable, Istate, where Istate = NCO >> 20. A quadrature version (cosine) ~~216~~ 218 is created by ~~a~~ digital delay ~~218~~ 216 to advance the Istate by four states (90-degrees). Qstate = (Istate + 4) & 0xF. The Istate and Qstate are both input to respective 16-state lookup tables 220 and 222, e.g., ---